distinction of being truly die-sized, not “chip scale.” For WLPs, underfill is typically not applied. Since there exists

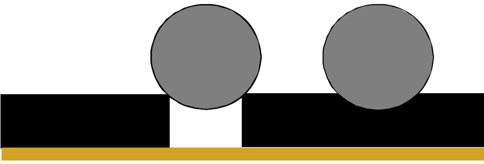

Figure 10. Polymer film/UBM delamination [15]

For wafer level packages, PCB is considered as 'part' of the package since one cannot decouple the PCB from the WLP. PCB design plays an important role to assess the reliability of WLPs. With the conventional JEDEC board test set up and design, PCB trace cracks were often obserm.4(B i.0613 pac)6.8(k)-21998 re 124 27052w.e asses PC952w.eesWeo si5th

between the silicon chip and PCB [19]. In Fig. 14, the per-cycle inelastic energy density is plotted against the location of solder balls in a diagonal direction for a 16×16 array fan-out WLP package, in which 6×6 array solder balls are under die area. Fig. 14 shows that outermost ball right beneath silicon die has the maximum inelastic energy density among all balls. This is because the maximum local CTE mismatch is between silicon chip and the PCB. Thus the thermal stresses of solder balls beneath the chip are expected to be higher than the stresses on the outermost solder balls. The results show that fan-out WLP packages can extend the array size greatly while meeting thermo-mechanical reliability requirement.

three stacking schemes in 3D integration: chip-to-chip, chip-to-wafer, and wafer-to-wafer. Wafer-to-wafer technology can be applied for homogeneous integration of high yielding devices. Wafer-to-wafer bonding maximizes the throughput, simplifies the process flow, and minimizes cost. The drawback for this wafer-to-wafer method is the number of known-good-die (KGD) combinations in the stacked wafers will not be maximized when the device wafer yields are not high enough or not stable. In this case, chip-to-chip or chip-to-wafer will be adopted to ensure vertical integration with only good dies. Considering mass production in future, the chip-to-wafer and wafer-to-wafer technologies have gradually become the mainstream for 3D integration.

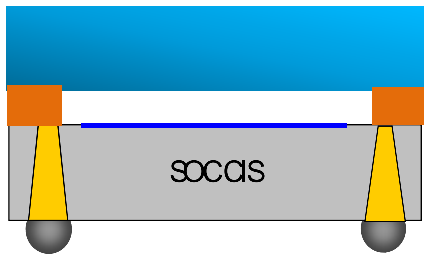

Figure 16. Image sensor WLP with TSV

Wafer-level bonding/bonding/stacking technologies can be further differentiated by the method used to create TSVs: either via-first or via-last. The common definition for via-first and via-last is based on TSVs formed before and after BEOL process. TSV fabrication after the wafers are bonded, using a ‘‘drill and fill” sequence, is definitely via-last approach. Whereas via-first and pre-bonding vialast approaches, building TSVs on each wafer prior to the bonding process are generally more efficient and cost-effective. The leading wafer-level bonding techniques used in 3D integration include adhesive bonding (polymer bonding), metal diffusion bonding, eutectic bonding, and silicon direct bonding [26]. The future development will reply on the full integration of fan-out technology, WLP, and vertical 3D interconnect technology together.

5. Conclusions

Conventional fan-in WLPs are a unique form of packages and have the distinction of being truly die-sized, not “chip-scale’. With fan-out WLP technologies emerging, expensive substrate process can be eliminated. For fan-in WLP, the RDL build-up stacks or copper post/epoxy stacks serve as stress buffer to reduce solder ball stresses significantly. However, the failure mode may shift to the failures in stack-up layers. For fan-out WLP, the die-size is no longer a limiting factor for WLP reliability. Instead, several challenges in wafer reconstitution process arise. Moisture sensitivity becomes a coneren in fan-out WLP development. The integration of fan-out (wafer reconstitution), WLP, and TSV will truly realize system integration in future.

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